REMARKS

Claims 2, 12, 17 and 21 have been cancelled. Claims 1, 9, 15, 19, and 23 have been amended. Claim 36 has been added. Claims 1, 3-11, 13-16, 18-20 and 22-36 remain pending in the application.

Claims 1, 3-7, 9-11, 13-16, 18-20, 22-24 and 31-35 over Miller in view of Li

In the Office Action, claims 1, 3-7, 9-11, 13-16, 18-20, 22-24 and 31-35 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 5,946,177 to Miller et al. ("Miller"), in view of U.S. Patent No. 6,639,771 to Li ("Li"). The Applicants respectfully traverse the rejection.

Claims 1, 3-7, 9-11, 13-16, 18-20, 22-24 and 31-35 recite a switchable low resistance path between a power rail and a ground rail, the low resistance path being adapted to be switched ON for a duration an electrical over stress ("EOS") event lasting significantly more than 2 microseconds, the EOS occurring during a difference in an order in which connections are made between contacts of a powered device and contacts of an unpowered device as they are connected or disconnected. In claims 1, 3-7, 9-11, 13-14, 19-20, 22-24, 31-32 and 34-35, the EOS event is detected by an EOS detector comprising a programmable element.

Miller appears to disclose a circuit for ESD protection during an ESD event. The circuit has a shunt device, a trigger circuit and a separate RC delay circuit. Col. 4, lines 47-48. The RC delay circuit serves to maintain the shunt device in the conductive state, initially produced by the trigger circuit, for the remaining duration of the ESD event. Col. 4, lines 54-58.

The Examiner states that Miller is directed to providing protection against both ESD and EOS events. Office Action, p. 8. While the field of Miller's invention includes both types of events, Miller's device is directed to a circuit providing ESD protection. Col. 4, lines, 44-47. In discussing the prior art, Miller discloses that "it is critical that this RC time constant is long enough to exceed the maximum expected duration of an ESD event, typically a few hundred nanoseconds, while short enough to avoid false triggering of the clamp circuit

during normal ram-up of the V_{DD} power rail, typically a few milliseconds." Col. 1, lines 47-51.

Figure 5 shows the operation of a clamp circuit disclosed in Miller during an ESD event. In explaining Figure 5, Miller states that the time constant of the RC delay circuit is set to about 1000 nanoseconds and that the V_{DD} rail circuits decays to V_{ss} over a period of about 500 nanoseconds. Col. 7, lines 1-2. There is nothing in Miller disclosing or suggesting that its circuit will protect against an EOS event lasting significantly longer than 2-3 microseconds.

The Examiner alleges that since the RC time constant disclosed in Miller is a result effective variable, one of ordinary skill in the art would have modified the RC time constant in Miller to protect against an EOS event. Office Action, pp. 8-9. The Applicants respectfully disagree. EOS events last substantially longer and involve more current than ESD events. ESD circuits have to be designed to protect circuits for this longer period of time and to handle the higher currents. Thus, Miller would not suggest to one skilled in the art circuitry designed to protect against ESD events, as recited by claims 1, 3-7, 9-11, 13-16, 19-20, 22-24 and 31-35. There is also nothing in Miller about the EOS event detector comprising a programmable element, as recited in claims 1, 3-7, 9-11, 13-14, 19-20, 22-24, 31-32 and 34-35.

The Examiner acknowledges that Miller did not disclose an EOS event occurring during a difference in an order in which connections are made between contacts of a powered device and contacts of an unpowered device as they are connected or disconnected. The Examiner relies on Li to remedy this deficiency.

Li, however, discloses an external EOS protection circuit that protects the internal ESD protection diode from failure during hot-swap insertion. Col. 3, lines 3-5. An external MOSFET is placed in series with the ground pin of the integrated circuit chip. The external MOSFET turns on after a delay when power is applied during hot insertion. Li thus does not disclose or suggest that an ESD event will last longer than 2-3 microseconds. Li further does not disclose or suggest a switchable low resistance path between a power rail and a ground

rail for EOS protection. Thus, even if Miller and Li are combined, the hypothetical combination does not disclose or suggest a switchable low resistance path between a power rail and a ground rail, the low resistance path being adapted to be switched ON for a duration an electrical over stress lasting significantly more than 2 microseconds, the electrical over stress occurring during a difference in an order in which connections are made between contacts of a powered device and contacts of an unpowered device as they are connected or disconnected,. as recited by claims 1, 3-7, 9-11, 13-16, 19-20, 22-24 and 31-35. Miller and LI also do not disclose an EOS event detector comprising a programmable element, as recited in claims 1, 3-7, 9-11, 13-14, 19-20, 22-24, 31-32 and 34-35.

Moreover, Li is directed to protecting against the internal ESD protection diode from failure during hot-swap board insertion. Col. 3, lines 3-5. It does not disclose protecting against an EOS event caused by other procedures, such as inserting a Firewire cable, as recited by claims 1, 3-7, 9-11, 13-16, 19-20, 22-24 and 31-35.

Accordingly, for at least all the above reasons, claims 1, 3-7, 9-11, 13-16, 19-20, 22-24 and 31-35.are patentable over the prior art of record. It is therefore respectfully requested that the rejection of these claims be withdrawn.

Claims 8 and 25-35 over Miller in view of Li and further in view of Whitney

In the Office Action, claims 8 and 25-35 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Miller in view of Li and further in view of U.S. Patent Application Publication No. 2002/0024791 to Whitney et al. ("Whitney"). The Applicants respectfully traverse the rejection.

Claims 8 and 26 are dependent on independent claim 1. Claims 25 and 30 are dependent on independent claim 23. Claim 27 is dependent on independent claim 9, claim 28 is dependent on independent claim 15 and claim 29 is dependent on independent claim 19. Claims 8 and 25-30 are patentable for the same reasons that the corresponding independent claims are patentable over the prior art of record.

Claims 8 and 25 contain the additional limitation that the integrated circuit includes a Firewire IEEE 1394 interface. Claims 26-30 contain the additional limitation that one of the powered device and the unpowered device is a cable. The Examiner acknowledges that the combination of Miller and Li does not disclose these limitations. The Examiner cites to Whitney to remedy this deficiency.

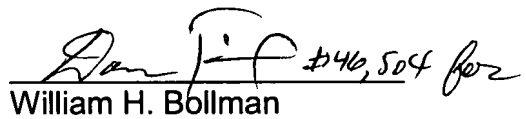
Whitney appears to disclose a system and method of protecting devices from ESD events and over-current conditions (See paragraph 0002). A varistor 302 is shown as attached between a power source Vin and GND (See Whitney, Fig. 11, paragraph 0091). Thus, Whitney does not disclose or suggest any type of switchable path between a power rail and a ground rail. Thus, the theoretical combination of Miller, Li and Whitney does not disclose or suggest a switchable low resistance path between a power rail and a ground rail, the low resistance path being adapted to be switched ON for a duration of a electrical over stress event lasting significantly more than 2-3 microseconds, the electrical over stress event occurring during a difference in an order in which connections are made between contacts of a powered device and contacts of an unpowered device as they are connected or disconnected, as recited by claims 8 and 25-35. Miller, LI and Whitney also do not disclose an EOS event detector comprising a programmable element, as recited in claims 8, 25-27, 29-32 and 34-35.

Accordingly, for at least all the above reasons, claims 8 and 25-35 are patentable over the prior art of record. It is therefore respectfully requested that the rejection of these claims be withdrawn.

Conclusion

All rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,



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